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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,217	01/18/2002	Hussein S. El-Ghoroury	005444.P005	7189

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER

MITCHELL, JASON D

ART UNIT	PAPER NUMBER
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2193

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/051,217

Applicant(s)

EL-GHOROURY, HUSSEIN S.

Examiner

Jason Mitchell

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 January 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>4/11/02</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This application claims priority to U.S. provisional applications 60/262803 and 60/268835 filed on 1/19/01 and 2/13/01, respectively.
2. Claims 1-19 are pending in this case.

Specification

The disclosure is objected to because of the following informalities: Many references to the drawings are miss labeled. For example on pg. 13 references to Fig. 3A give reference numbers in the 200's (e.g. 225) while the drawing is labeled with numbers in the 100's (e.g. 125). Applicant's cooperation is requested in detecting and correcting any errors of this nature of which applicant may become aware.

Claim Objections

3. **Claim 16 objected to because of the following informalities:** Claim 16 contains an extra period, one in line 3 and one in line 5. Individual claims are required to consist of exactly one sentence (See *Fressola v. Manbeck*, 36 USPQ2d 1211 (D.D.C. 1995)). Appropriate correction is required.
4. **Claim 17 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim.** Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Both claim 16

and 17 recite the limitation of using 'the interconnect design vectors to contain connectivity characteristics of the processing pipeline'.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claim 12 recites the limitation "the behavioral model" in line 2. There is insufficient antecedent basis for this limitation in the claim.** For the purposes of this examination, the "behavioral model" will be assumed to be a behavioral model as recited in claim 11.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-8 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The language of the claims raises a question as to whether the claim is directed merely to an abstract idea that is not tied to a technological art, environment or machine which would result in a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 U.S.C. 101. Claim 1 recites analyzing a design specification, decomposing a processor system and analyzing the resulting interconnected design

vectors. The claim does not explicitly recite the use of a tangible media, nor do any of the limitations appear to necessitate such a medium. The dependent claims do not correct this deficiency.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. **Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,867,400 to El-Ghoroury et al. (El-Ghoroury) in view of US 6,484,304 to Ussery et al. (Ussery).**

Regarding Claims 1, 9, 19: El-Ghoroury discloses a method to efficiently design and implement a matched instruction set processor system, including: analyzing and mapping design specifications of the matched instruction set processor into application components (col. 3, lines 47-51 'analyzes the design requirements ... and describes them in terms of a subset of application specific function blocks'), each application component representing a reusable function commonly used in digital communication systems (col. 3, lines 47-51 'application specific function blocks selected from the library'); decomposing the matched instruction set processor system into interconnected design vectors (col. 9, lines 34-37 'decomposed into fundamental application specific processes'), and analyzing and mapping the interconnected design vectors into specific

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hardware and software elements (col. 10, lines 1-2 'the design is released for ASIC layout and fabrication'). El-Ghoroury does not explicitly disclose the interconnected design vectors are represented in Java programming language

Ussery discloses using Java programming language to represent design vectors (col. 3, lines 10-14 'high-level language ... such as Java') in an analogous art for the purpose of 'producing a custom integrated circuit' (col. 2, lines 52-55).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Ussery's task data vector representation (col. 3, lines 10-14 'high-level language ... such as Java') in El-Ghoroury's invention in order to incorporate Ussery's optimizations (Ussery col. 6, lines 15-18 'optimize the control flow')

Regarding Claims 2, 10: The rejections of claims 1 and 9 are incorporated, respectively; further El-Ghoroury discloses performing a behavioral analysis of the matched instruction set processor system to ensure compliance with the design specifications (col. 9, lines 52-54 'ascertain whether the ... interfaces are compliant with the design specifications').

Regarding Claims 3, 11, 12: The rejections of claims 1, 9 and 9 are incorporated, respectively; further El-Ghoroury discloses performing a requirement analysis of the design specifications of the matched instruction set processor system to generate a behavioral model (col. 9, lines 52-54 'Behavioral level simulation is performed'); and representing the behavioral model using application components (col. 3, lines 47-51 'application specific function blocks selected from the library').

Regarding Claims 4, 13: The rejection of claims 1 and 9 are incorporated, respectively; further El-Ghoroury discloses mapping the application components into corresponding architectural components (col. 9, line 67-col. 10, line 2 'the design is released for ASIC layout and fabrication').

Regarding Claims 5, 14: The rejections of claims 4 and 13 are incorporated, respectively; further El-Ghoroury does not explicitly disclose decomposing each application component into processing pipelines to satisfy system processing and timing requirements.

Ussery discloses decomposing each application component into processing pipelines to satisfy system processing and timing requirements (col. 6, lines 48-54 'partitioned into microtasks taking into consideration ... opportunities for software pipelining').

Regarding Claims 6, 15: The rejections of claims 5 and 14 are incorporated, respectively; further El-Ghoroury does not explicitly disclose decomposing each processing pipeline into design vectors, including functional design vectors and interconnect design vectors.

Ussery discloses decomposing each processing pipeline into design vectors, including functional design vectors and interconnect design vectors (col. 6, lines 41-47 'decompose tasks into threads then through dataflow analysis, decompose the threads into microtasks').

Regarding Claims 7, 16, 17: The rejections of claims 6, 15 and 15 are incorporated, respectively; further El-Ghoroury does not explicitly disclose using the functional design vectors to represent design information for at least one functional aspect of the

processing pipeline and using the interconnect design vectors to contain connectivity characteristics of the processing pipeline.

Ussery discloses using the functional design vectors to represent design information for at least one functional aspect of the processing pipeline (col. 5, lines 2-4 'Each microtask is a ... program for a target task engine'); and using the interconnect design vectors to contain connectivity characteristics of the processing pipeline (col. 6, lines 49-52 'partitioned into microtasks taking into consideration ... flow of control').

Regarding Claims 8, 18: The rejections of claims 7 and 17 are incorporated, respectively; further El-Ghoroury discloses decomposing the matched instruction set processor system into interconnected design vectors further includes: providing in each design vector, a run method (col. 3, lines 4-6 'engines that executes microtask instructions'), a Java virtual machine (JVM) (col. 6, lines 64-67 'A microtask analyzer and code generator'), and an invocation method (col. 3, lines 4-6 'engines that executes microtask instructions') and inherently discloses a binding header method and a binding trailer method (col. 3, lines 28-30 'the compiler may insert direct memory data references in each of the microtasks').

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11

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F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-19 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-19, respectively, of copending Application Nos. 10/051,535 (535) and 10/052312 (312). Although the conflicting claims are not identical, they are not patentably distinct from each other because:

The only distinction between the instant claims and those of the 535 and 312 references, is the recitation 'the interconnected design vectors are represented in Java programming language' in claims 1, 9 and 19 of the instant application; and the recitation of 'Java virtual machine (JVM)' from the instant application in place of 'conjugate virtual machine' from the 535 and 312 references.

Both Java programming language and the Java virtual machine were well known in the art at the time of the invention and it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement an application as described in the 535 and 312 references using Java programming language and the Java virtual machine.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claims 1, 9 and 19 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 11 and 21 of copending Application No. 10/156,170 (170). Although the conflicting claims are not identical, they are not patentably distinct from each other because: Claims 1, 11 and 21 of the 170 reference are identical to 1, 9 and 19 of the 535 and 312 references discussed above. Consequently claims 1, 9 and 19 of the instant application are rejected on the same grounds with respect to the 170 reference.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Mitchell whose telephone number is (571) 272-3728. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jason Mitchell
6/23/05



ANIL KHATRI
PRIMARY EXAMINER